

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): R. Scott LIST et al.
Serial No.: Divisional of Application No. 10/066,668
filed on February 6, 2002
Filed: July 7, 2003
For: A BARRIER STRUCTURE AGAINST CORROSION AND CONTAMINATION
IN THREE-DIMENSIONAL (3-D) WAFER-TO-WAFER VERTICAL STACK
Group: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97 & §1.98

Assistant Commissioner of Patents
Washington, D.C. 20231

July 7, 2003

Sir:

In the matter of the above-identified application, this Information Disclosure Statement is being submitted with the following citation as specified in 37 CFR §1.97(d).

"A copy of any patent, publication or other information listed in an Information Disclosure Statement is not required to be provided if it was previously cited by or submitted to the Office in a prior application, provided that the prior application is properly identified in the statement and relied upon for an earlier filing date under 35 U.S.C. §120."

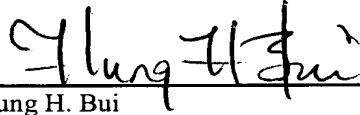
Applicant(s) are submitting herewith a copy of Form PTO-1449 which list documents cited in parent application(s) Serial No. 10/066,668, filed February 6, 2002.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit

Account No. 01-2135 (219.40603VX1) please credit any excess fees to such deposit account.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Hung H. Bui", is written over a solid horizontal line.

Hung H. Bui

Registration No. 40,415

ANTONELLI, TERRY, STOUT & KRAUS, LLP

HHB/slh

Substitution for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Filing Date	July 7, 2003
				First Named Inventor	R. Scott LIST
				Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	1	of	2	Attorney Docket Number	219.40603VX1

[illegible][illegible]

Examiner Signature		Date Considered	
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¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:** Assistant Commissioner for Patents, Washington, DC 20231.

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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Divisional of Application No. 10/066,668
				Filing Date	July 7, 2003
				First Named Inventor	R. Scott LIST
				Group Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	219.40603VX1

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		"Ultra Thin Electronics for Space Applications", 2001 Electronic Components and Technology Conference, 2001 IEEE	
		Copper Wafer Bonding"; A. Fan, A. Rahman, and R. Reif; Electrochemical and Solid-State Letters, 2 (10) 534-536 (1999)	
		"Face to Face Wafer Bonding for 3D Chip Stack Fabrication to Shorten Wire Lengths", June 27-29, 2000 VMIC Conference 2000 IMIC – 200/00/0090(c)	
		"InterChip Via Technology for Vertical System Integration", Fraunhofer Institute for Reliability and Microintegration, Munich, Germany; Infineon Technologies AG, Munich, Germany; 2001 IEEE	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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